

REMARKS/ARGUMENTS

In the Office Action mailed February 27, 2008, claims 1-6 were rejected. In response, Applicants have amended claims 1-3 and 6. Applicants hereby request reconsideration of the application in view of the amended claims and the below-provided remarks. No claims have been added or canceled.

Claim Rejections under 35 U.S.C. 112

Claims 1-6 are rejected under 35 U.S.C. 112 as failing to comply with the written description requirement. In response, Applicants have amended claims 1-3 and 6. Applicants respectfully assert that claims 1-6 meet the requirements of 35 U.S.C. 112. In particular, the amendments replace the term “respective analog control signal” with the term “respective control signal”, the term “combining” with the term “summing”, and the term “continuously variable combined analog control signal” with the term “summed control signal”. Support for the amendments is found in Applicants’ specification at, for example, paragraphs [0052] and [0072].

Claim Rejections under 35 U.S.C. 102 and 103

Claims 1-2 and 5-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Elappuparackal et al. (U.S. Pat. No. 6,822,478, hereinafter Elappuparackal). Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Elappuparackal in view of Gasztonyi (U.S. Pat. No. 5,339,445). However, Applicants respectfully submit that these claims are patentable over Elappuparackal and Gasztonyi for the reasons provided below.

Independent Claim 1

Claim 1 has been amended to particularly point out that control signals are summed to form a summed control signal and to particularly point out that “an analog level of said summed control signal is the sum of analog levels of said respective control signals”. Support for the amendments is found in Applicants’ specification at, for example, paragraphs [0052] and [0072]. As amended claim 1 recites:

“An electronic circuit comprising:

a plurality of sequential logic elements, each one of the sequential logic elements comprising:

at least one clock terminal for receiving a clock signal;

at least one input terminal for receiving an input signal;

at least one output terminal for providing an output signal;

circuitry, for monitoring said input and output signals of respective sequential logic elements to provide respective control signals in response to said input and output signals of said respective sequential logic elements; and

means for summing said respective control signals to form a summed control signal, wherein an analog level of said summed control signal is the sum of analog levels of said respective control signals, and controlling a power consumption of the electronic circuit in response to said summed control signal.”
(emphasis added).

In contrast to amended claim 1, Elappuparackal does not disclose the “means for summing said respective control signals to form a summed control signal, wherein an analog level of said summed control signal is the sum of analog levels of said respective control signals”, as recited in amended claim 1. In particular, Elappuparackal discloses that respective control signals from exclusive OR gates (140-143) are combined by OR gates (45-47) to produce a single output, LD (see Figure 5, column 5 lines 39-58, and column 6 lines 11-21 of Elappuparackal). The current level and the voltage level of the single output, LD, is related to the parameters of the OR gates (45-47) and to the result of the logic operations of respective control signals from the exclusive OR gates (140-143). However, the current level and the voltage level of the single output, LD, is not the sum of the analog current and voltage levels of the respective control signals from the exclusive OR gates (140-143). Although Elappuparackal may disclose an electronic circuit including a plurality of sequential logic elements, circuitry for monitoring input and output signals of respective sequential logic elements, and means for controlling power consumption of the electronic circuit, Applicants respectfully assert that Elappuparackal does not disclose the “means for summing said respective control signals to form a summed control signal, wherein an analog level of said summed control signal is the sum of analog levels of said respective control signals”, as recited in amended claim 1.

Because Elappuparackal does not disclose the “means for summing said respective control signals to form a summed control signal, wherein an analog level of

said summed control signal is the sum of analog levels of said respective control signals”, Applicants respectfully assert that amended claim 1 is not anticipated by Elappuparackal.

Dependent Claims 2-5

Applicants have amended claims 2 and 3 to clarify the phrases. Claims 2-5 are dependent on claim 1. Applicants respectfully assert that claims 2-5 are allowable at least based on an allowable claim 1.

Independent Claim 6

Claim 6 has been amended to particularly point out “summing said respective control signals to form a summed control signal, wherein an analog level of said summed control signal is the sum of said respective control signals”. Support for the amendment is found in Applicants’ specification at, for example, paragraphs [0052] and [0072].

Claim 6, as amended, includes similar limitations to amended claim 1. In view of the amendments to claim 6, Applicants respectfully assert that remarks made above with regard to amended claim 1 apply also to amended claim 6.

CONCLUSION

Applicants respectfully request reconsideration of the claims in view of the amendments and the remarks made herein. A notice of allowance is earnestly solicited.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-3444** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-3444** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

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Respectfully submitted,

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